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# Bias Voltage Effect on Electrical Properties of N-type Polymeric Field Effect Transistors with Dual Gate Electrodes

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*We investigated the bias voltage effect on the electrical properties of n-type polymer field-effect transistors (FETs) with dual gate electrodes. The electrical characteristics of such polymer FETs were measured as a function of the sweeping voltage at one gate electrode when the other gate electrode was floated or biased. The hysteresis was negligible when the top gate voltage was swept while the bottom gate was biased. The threshold voltage decreases and the mobility increases with increasing the bottom gate bias due to the increase of mobile charges.*

**Keywords** Dual gate; organic field-effect transistor; n-type polymer semiconductor; threshold voltage

## Introduction

Polymer field-effect transistors (FETs) have attracted much attention for their potential use in flexible, low-cost electronic circuits [1–3]. In order to improve the electrical properties of the polymer FETs such as the on-current and the subthreshold swing, dual gate configurations of the polymer FETs have been proposed [4–7]. Among them, p-type polymer FETs have been quite extensively studied while n-type polymer FETs required for complementary circuits are barely demonstrated due to lack of proper materials.

In this study, we investigated the bias voltage effect on the electrical properties of n-type polymer FETs with dual gate electrodes. Their electrical characteristics including the hysteresis, the mobility, and the threshold voltage were measured as a function of the sweeping voltage at one gate electrode under the condition that the other gate was floated or biased.

## Experimental Consideration

The cross-sectional view of our dual gate configuration of n-type polymer FETs is schematically shown in Fig. 1(a). A p-doped Si substrate and a layer of 300 nm-thick $SiO_2$ were

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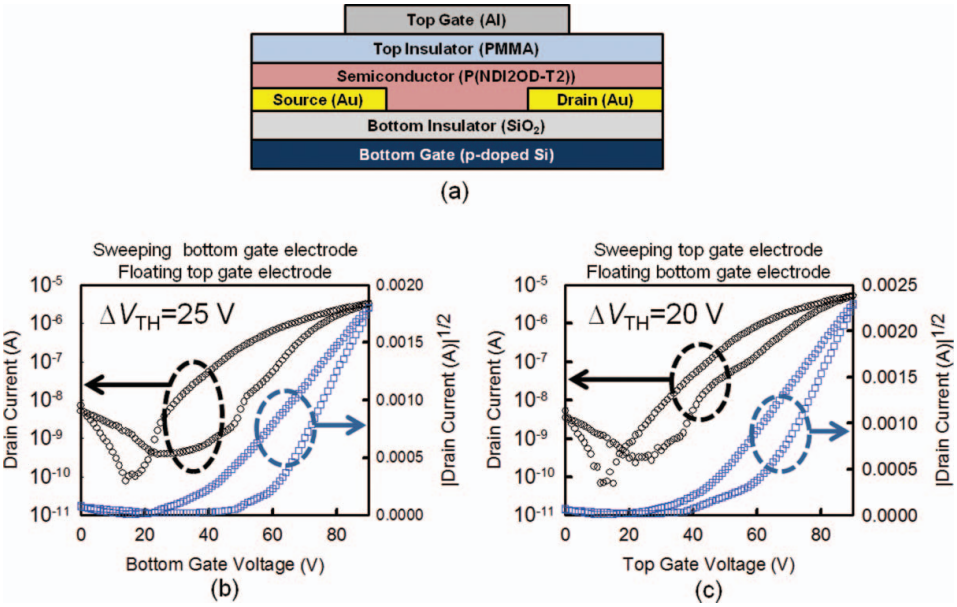


**Figure 1.** A schematic cross-sectional view of the n-type polymer FET with dual gate electrodes (a). The transfer characteristic curves (circles) and the square root of the drain current (squares) on sweeping the bottom gate voltage when the top gate is floated (b) and those on sweeping the top gate voltage when the bottom gate is floated (c).

used for the bottom gate electrode and an insulator, respectively. The $Si/SiO_2$ substrate was cleaned with acetone, isopropyl alcohol, methanol, and deionized water in series for ten minutes each. The cleaned $Si/SiO_2$ substrate was exposed to UV-ozone and immersed in the toluene solution with octadecyltrichlorosilane to form a self-assembled monolayer on the surface of $SiO_2$ for improving the charge transport. The source and drain electrodes were prepared using 50-nm-thick Au by thermal deposition. The channel length and width were 80 $\mu$m and 1 mm, respectively. Poly{[N,N9-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,59-(2,29-bithiophene)} [P(NDI2OD-T2)], dissolved in dichlorobenzene in 1 wt.%, was used to form an organic semiconductor layer by spin-coating at 3000 rpm for 30 sec and subsequently baked at 110°C for overnight in a vacuum dry oven. In preparing a top gate insulator, poly(methyl methacrylate) (PMMA) dissolved in ethyl acetate in 8 wt.% was spin-coated at 3000 rpm for 30 sec and baked at 100°C for 1 hour. The thickness of the PMMA film was 1.8 $\mu$m. The top gate electrode of 50-nm-thick Al was thermally deposited. Electrical characteristics of our polymer FETs with dual gate electrodes were measured at room temperature under ambient condition using a semiconductor analyzer (HP 4155A).

## Results and Discussion

We first examine the bias voltage effect on the hysteresis behaviors of n-type polymer FETs with dual gate electrodes. Figures 1(b) and (c) show the transfer characteristics as a function of the sweeping voltage at one gate electrode when the other gate was floated and vice versa, respectively. The hysteresis, which is defined as the difference (or the shift) of the threshold voltage between the forward sweeping (the gate voltage from 0 to 90 V) and the

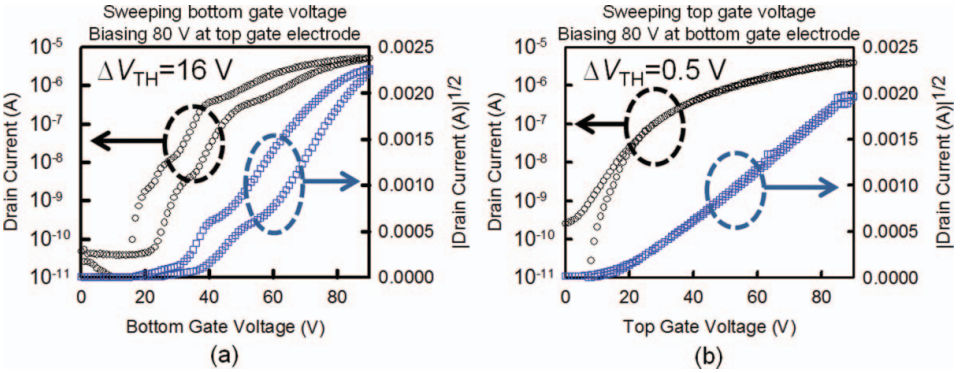


**Figure 2.** The transfer characteristic curves (circles) and the square root of the drain current (squares) on sweeping the bottom gate voltage when the top gate is biased (a) and those on sweeping the top gate voltage when the bottom gate is biased (b) at the drain voltage ($V_D$) of 50 V.

backward sweeping (the gate voltage from 90 to 0 V), was determined to be 24.6 V during sweeping the bottom gate voltage as shown in Fig. 1(b) while it was 20.2 V during sweeping the top gate voltage in Fig. 1(c). This large hysteresis results from the high trap density in the polymer semiconductor layer. In fact, the hysteresis originates from the change in the number of the trapped charges in the semiconductor layer during sweeping the gate voltage [8].

We now describe the transfer characteristics of our n-type polymer FETs as a function of the sweeping voltage at one gate electrode under the condition that the other gate was biased and vice versa. As shown in Figs. 2(a) and (b), the hysteresis was 15.5 V during sweeping the bottom gate voltage when the bias voltage was 80 V at the top gate electrode as shown in Fig. 2(a). For the case that the top gate and the bottom gate were interchanged, the hysteresis was found to be 0.5 V as shown in Fig. 2(b). This large difference of the hysteresis seen in Figs. 2(a) and 2(b) indicates that the trap density in the bottom channel is much higher than that in the top channel. Under the circumstance that the bottom gate voltage is swept for the bias voltage at the top gate electrode, only the number of the trapped charges in the bottom channel is changed while that in the top channel remains constant. This is also valid for the case that the top gate and the bottom gate are interchanged.

Let us discuss the effect of the magnitude of the bias voltage on the transfer characteristics of the n-type polymer FETs during sweeping the voltage at one gate electrode when the bias voltage is applied to the other gate electrode and vice versa. The transfer characteristic curves on sweeping the bottom gate voltage when the bias voltage at the top gate electrode was varied from 0 to 80 V are shown in Fig. 3(a). At the bias voltage of 0 V, no transfer characteristics were available. Above the bias voltage of 20 V, typical n-type transfer characteristic curves were observed. During sweeping the bottom gate voltage, the on-current increases from 46 nA to 5.1 $\mu$A at 90 V with increasing the bias voltage at the top gate electrode from 20 to 80 V as shown in Fig. 3(a). One interesting point is that the transfer characteristic curves are quite crooked and become shifted toward increasing the on-current with increasing the bias voltage at the top gate electrode. The capacitance of the bottom gate insulator is about six times larger than that of the top gate insulator. With increasing the bottom gate voltage, while the electrons in the bottom channel are accumulated, those in the top channel pre-accumulated by the top bias voltage become depleted. This is why the transfer curves were crooked.

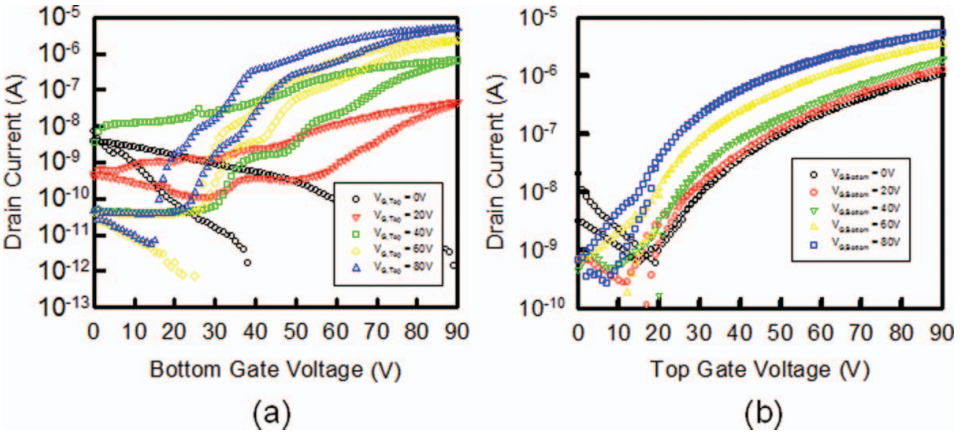


**Figure 3.** The transfer characteristic curves on sweeping the bottom gate voltage when the bias voltage at the top gate electrode is varied (a) and those on sweeping the top gate voltage when the bias voltage at the bottom gate electrode is varied (b) at $V_D = 50$ V.

When the top gate electrode and the bottom gate electrode are interchanged, the on-current increases from 1.0 to 5.6 $\mu$A at 90 V with increasing the bias voltage at the bottom gate electrode from 0 to 80 V as shown in Fig. 3(b). Note that in this case, the hysteresis was negligible and no crooked behavior was observed in the entire range of the bias voltage we studied. Again, the transfer characteristic curves were shifted toward increasing the on-current with increasing the bias voltage.

Finally, the mobility and the threshold voltage in our p-type polymer FET are plotted as a function of the bias voltage at the bottom gate electrode in Fig. 4. The threshold voltage decreases with increasing the bias voltage at the bottom gate electrode. It was shifted from 38 to 19 V with increasing the bias voltage from 0 to 80 V. In contrast to the

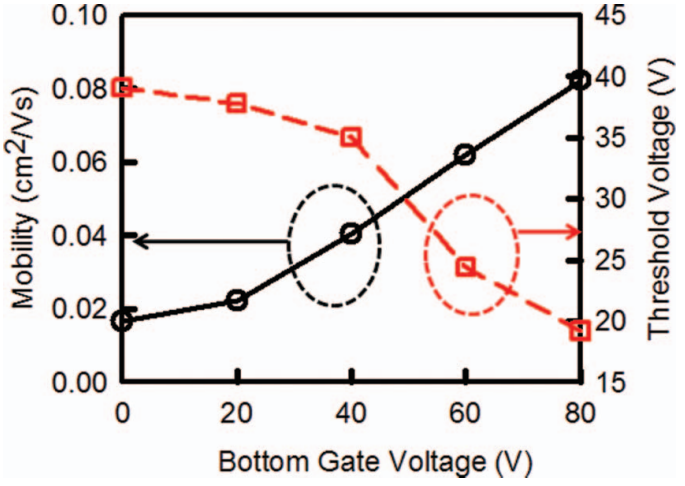


**Figure 4.** The mobility and the threshold voltage in our n-type polymer FET with dual gate electrodes as a function of the bias voltage at the bottom gate electrode.

p-type polymer FET with dual gate electrodes whose threshold voltage is positively shifted with increasing the negative bias voltage [7], our n-type polymer FET exhibits a negative shift of the threshold voltage with increasing the positive bias voltage since the electron is the majority carrier in the n-type semiconducting polymer. The mobility increases almost linearly from 0.017 to 0.082 $cm^2$/Vs with increasing the bottom gate voltage from 0 to 80 V. The behaviors of the threshold voltage and the mobility in the presence of the bias voltage are attributed to the enhanced injection of mobile electrons from the source electrode to the n-type semiconducting polymer.

## Conclusions

We demonstrated how the bias voltage affects the electrical characteristics of n-type polymer FETs with dual gate electrodes. The hysteresis is primarily governed by which gate electrode (bottom or top) is swept or biased. In our case, the hysteresis is negligible only when the top gate voltage is swept under the condition that the bottom gate electrode is biased. The dual gate configuration of the n-type polymer FET presented here will be useful for constructing a variety of organic integrated circuits.



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